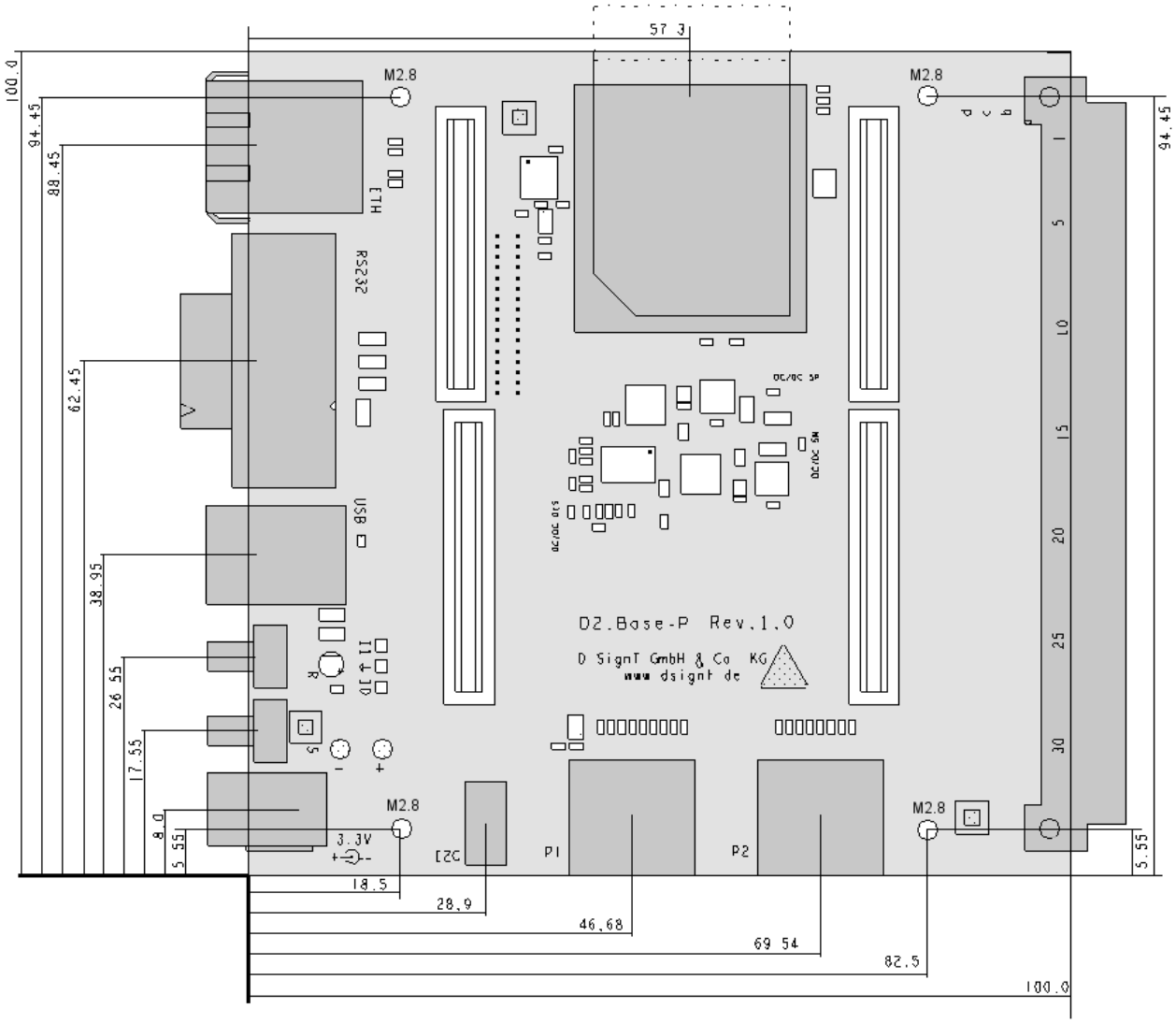
D2.Base-P

Board Revision 1.0 **Document Revision 0.3 Preliminary** **Apr 22, 2016**



Features

- 100x100mm base board for D.Module2 evaluation, accepts DSP, FPGA, and Analog-I/O board stacks
- 3.3V single supply, +/-5V rails for data acquisition daughter cards generated on-board
- Ethernet, RS232, USB and SD card Connectors
- I²C, SPI, and GPIO Pmod™ compatible connectors (Pmod is a Digilent Inc. trademark)
- Expansion Interface with parallel bus and serial interface signals

Power Supply

The D2.Base requires an external 3.3V supply, connected to the DC jack. Alternatively 3.3V can be supplied via the External Bus Port pins 3.3V and 0V, or by two solder pads next to the DC jack.

An on-board switch mode converter generates +/-5V supply voltage for analog I/O daughter cards. The maximum output current is 600mA on the +5V rail, and 300mA on the -5V rail. If the analog power should be sourced from an external supply close solder jumpers DCDC_DIS and open jumpers DCDC_5P and DCDC_5M. Now you can connect an external supply to the External Bus Port pins AVPOS, AVNEG, AGND.

Pmod™

The Pmod connectors are used to connect low I/O pin count peripherals to the DSP board. By using Pmod peripherals (available from Digilent, Analog Devices, Maxim, and others), the DSP system is easily expanded with a display, keyboard, WiFi, low sampling rate A/D and D/A converters, etc.

Pmod I²C

This 2x4 pin header is used for I²C compatible peripherals. The VCC power supply is 3.3V. Pull-up resistors for SCL and SDA are already provided by the D.Module2 DSP board.

Pin	Signal	Signal	Pin
1	SCL	SCL	2
3	SDA	SDA	4
5	GND	GND	6
7	VCC	VCC	8

Table 1: Pmod I²C

Pmod Type 2A (Expanded SPI)

The 2x6 header P1 is used for SPI compatible peripherals. It accepts either an expanded SPI peripheral using both connector rows, or a standard SPI peripheral in the upper connector row plus a GPIO peripheral in the lower connector row.

Pin	6	5	4	3	2	1
Signal	VCC	GND	SCK	MISO	MOSI	SS_N
Pin	12	11	10	9	8	7
Signal	VCC	GND	IO4	IO3	IO2/ RESET	IO1 / INT

Table 2: Pmod Type 2A (expanded SPI)

The IO signals are connected to the D.Module2 DSP PRGIO signals, which can be individually configured as input or output:

IO1 / INT - PRGIO[8]
IO2 / RESET - PRGIO[9]
IO3 - PRGIO[10]
IO4 - PRGIO[11]

The active-low Slave Select (SS_N) is driven by the DSP PRGIO[12] signal, OR'ed with the DSP SPI Slave Select Output: PRGIO[12] must be configured as an output and driven low to activate SS_N during SPI transfers. PRGIO[12] must be driven high if other SPI peripherals are accessed, e.g. the SD/MMC card. The VCC power supply is 3.3V.

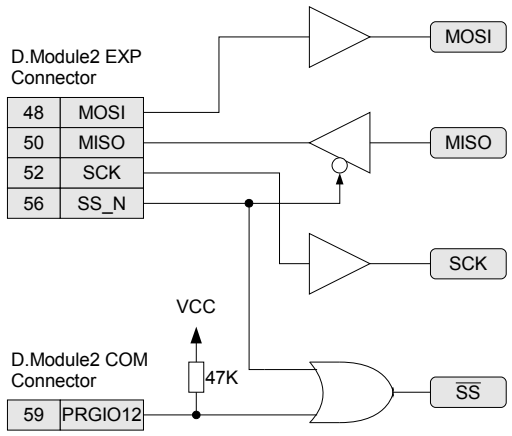


Figure 1: Pmod SPI Connections

Pmod Type 1 (GPIO)

The 2x6 header P2 accepts two standard GPIO peripherals or one expanded GPIO peripheral, e.g. a 4x4 keyboard.

Pin	6	5	4	3	2	1
Signal	VCC	GND	IO4_1	IO3_1	IO2_1	IO1_1
Pin	12	11	10	9	8	7
Signal	VCC	GND	IO4_2	IO3_2	IO2_2	IO1_2

Table 3: dual Pmod Type 1 (GPIO)

The IO signals are mapped to the D.Module2 PRGIO signals, which can be individually configured as input or output, the VCC power supply is 3.3V.

IO1_1 - PRGIO[0]
IO2_1 - PRGIO[1]
IO3_1 - PRGIO[2]
IO4_1 - PRGIO[3]
IO1_2 - PRGIO[4]
IO2_2 - PRGIO[5]
IO3_2 - PRGIO[6]
IO4_2 - PRGIO[7]

SD / MMC Card Slot

This card slot provides access to an SD or MMC non-volatile memory card for mass storage and data logging. The slot accepts standard size SD and MMC cards. Micro-SD cards can be used with an adapter.

The SD / MMC card is connected in SPI mode. DSP signals PRGIO[15..13] are used as control and status functions:
PRGIO[15] must be configured as an input and connects to the Card Detect (CD) signal (active low).
PRGIO[14] must be configured as an input and connects to the Write Protect (WP) signal (active low).
PRGIO[13] must be configured as an output. It is OR'ed with the DSP SPI slave select output and must be driven low to access the SD / MMC card. PRGIO[13] must be driven high on access to other SPI peripherals, e.g. the Pmod SPI interface. The SD/MMC card is powered with 3.3V.

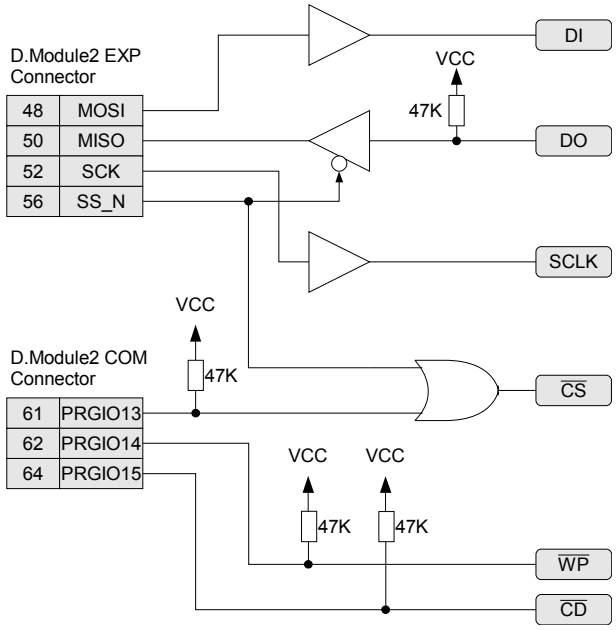


Figure 2: SD/MMC Card Connections

Ethernet / RS422 UART Connector

An RJ-45 8P8C connector on the front panel provides access to an Ethernet network. Optionally this connector can be used as an RS422 UART port.

Pin	1000Base-T	10/100Base-T	RS422
1	DA+	TX+	-
2	DA-	TX-	-
3	DB+	RX+	-
4	DC+	-	TxD+
5	DC-	-	TxD-
6	DB-	RX-	-
7	DD+	-	RxD+
8	DD-	-	RxD-

Table 4: RJ45 Ethernet / RS422 connector

The D.Module2 DSP boards are either equipped with a 1000Base-T Ethernet interface (Gigabit Ethernet), or with a 10/100Base-T Ethernet interface plus a RS422 UART. These interfaces share the same pins on the D.Module2 connector. Signal integrity requirements for 1000Base-T Ethernet do not allow add a dedicated RS422 connector to these signal traces. Therefore the signals to RJ45 pins 4,5 and 7,8 use DC blocking capacitors to prevent those DSP boards with an RS422 from disrupting the 1000Base-T interface.

The following diagram illustrates the RJ45 connections:

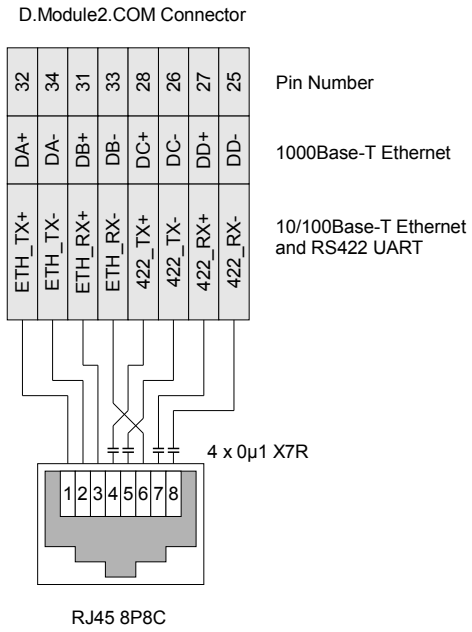


Figure 3: RJ45 Connections

If you use the 1000Base-T or 10/100Base-T Ethernet interface only, no modifications are required, simply connect the RJ45 connector to your Ethernet network.
In case you want to access the RS422 signals, replace the DC blocking capacitors with zero-ohms 0603 resistors. The DC blocking capacitors are located next to the RJ45 connector. If you want to use both 10/100Base-T Ethernet and RS422 simultaneously, build a Y-cable to split the RJ45 signals.

The currently available DSP boards support the following configurations:

DSP Board	1000Base-T	10/100Base-T	RS422
D.Module2.C6657	√	√	-
D.Module2.C6747	-	√	√
D.Module2.DM642	-	√	√
D.Module2.TS203	-	-	√

Table 5: DSP boards - Ethernet / RS422 configurations

RS232 UART Connector

This D-Sub 9-pin female connector is the default UART port of the D.Module2 DSP card. The connector includes Null-Modem wiring to allow direct access from a PC RS232 terminal with a 1:1 cable.

Pin	Signal
1	DCD – connected to pin 4 and 6
2	DSP TxD data output
3	DSP RxD data input
4	DTR – connected to pin 1 and 6
5	GND
6	DSR – connected to pin 1 and 4
7	DSP CTS hardware handshake input
8	DSP RTS hardware handshake output
9	RI – not used

Table 6: RS232 connector

USB Connector

The USB B-type device connector accesses the DSP card USB port. No power is drawn from the VBUS line.

Pin	Signal
1	VBUS
2	D-
3	D+
4	GND

Table 7: USB connector

Power Connector

This is a standard DC jack with 5.5mm sleeve diameter and a 2mm center tip. The power supply must be 3.3V DC. Alternatively power can be supplied via two solder pads with 1.5mm drill holes located next to the DC jack, labeled + (+3.3V) and – (0V), or via the External Bus Port pins 3.3V and 0V

Pin	Signal
Sleeve	0V
Tip	3.3V

Table 8: DC power connector

Reset and Setup Push Buttons

The push button next to the power jack is the Setup button, the one next to the USB connector is the Reset button. To force a hardware reset and a DSP re-boot, push the reset button. To enter the D.Module2 Setup (update and maintenance) mode keep the Setup button pressed while pushing and releasing the Reset button. Setup Mode requires a RS232 UART or USB terminal connection, Please refer to the D.Module2 User's Guide.

Power LED

The LED next to the Reset push button is lit if power is supplied to the base board.

IN0 and IN1

Three additional pins are located next to power jack: IN0, GND, and IN1. A standard 2.54mm jumper can be used to connect IN0 or IN1 to GND. IN0 is used on the D.Module2 DSP boards to force the Recovery Mode, which allows to update the BIOS firmware: Connect IN0 to GND with a jumper and enter Setup Mode. The DSP card now accepts a firmware update via the RS232 UART port. For normal operation leave IN0 open. IN1 can be used for user-defined purposes.

External Bus Port

The D.Module2 DSP external parallel bus and synchronous serial ports are available on the external bus header. No connector is attached to this port. Depending on your requirements a DIN41612 64ab, 96abc or 128 abcd connector can be mounted. Alternatively you can use standard 2.54mm pitch headers as a signal breakout.

Pin Number	Row a	Row b	Row c	Row d
1	FSR1	GND	FSX1	GND
2	CLKR1	GND	CLKX1	GND
3	DATR1	GND	DATX1	GND
4	FSR0	GND	FSX0	GND
5	CLKR0	GND	CLKX0	GND
6	DATR0	GND	DATX0	GND
7	GND	GND	GND	GND
8	GPIO0	GPIO2	GPIO1	GPIO3
9	D30	D14	D31	D15
10	D28	D12	D29	D13
11	D26	D10	D27	D11
12	D24	D8	D25	D9
13	D22	D6	D23	D7
14	D20	D4	D21	D5
15	D18	D2	D19	D3
16	D16	D0	D17	D1
17	GND	GND	GND	GND
18	A18	A14	A19	A15
19	A16	A12	A17	A13
20	A4	A10	A5	A11
21	A2	A8	A3	A9
22	A0	A6	A1	A7
23	GND	GND	GND	GND
24	CS0_N	GND	CS1_N	BE3_N
25	RD_N	OE_N	WR_N	BE2_N
26	WAIT_N	GND	RESOUT_N	BE1_N
27	IN0_N	INT2_N	INT1_N	BE0_N
28	BUSCLK	GND	GND	GND
29	3.3V	3.3V	3.3V	3.3V
30	0V	0V	0V	0V
31	AGND	AGND	AGND	AGND
32	AVNEG	AVNEG	AVPOS	AVPOS

Table 9: External Bus connector – DSP signals

If a D.Module2.6SLX45T FPGA board is mounted below the DSP card, the following FPGA signals are available on the external bus connector. IO cell pairs denoted with a P and N are routed as differential pairs to provide an LVDS link to the FPGA. These signals may also be used in a single-ended configuration. Signals marked gray are shared with DSP board signals. If using these signals please consult the DSP and FPGA board manuals to avoid collisions.

Pin	Row a	Row b	Row c	Row d
1	IO_L70N_1 [R16]	GND	IO_L72N_1 [T17]	GND
2	IO_L60N_1 [P16]	GND	IO_L73N_1 [T18]	GND
3	IO_L71P_1 [P17]	GND	IO_L70P_1 [R15]	GND
4	IO_L5N_0 [A3]	GND	IO_L1N_0 [D3]	GND
5	IO_L3P_0 [B2]	GND	IO_L1P_0 [C3]	GND
6	IO_L5P_0 [B3]	GND	IO_L3N_0 [A3]	GND
7	GND	GND	GND	GND
8	IO_L59P_2 [R9]	IO_L64N_0 [A19]	IO_L59N_2 [R8]	IO_L50N_0 [A17]
9	IO_L22N_2 [T11]	IO_L33P_0 [H10]	IO_L46N_2 [U10]	IO_L33N_0 [H11]
10	IO_L22P_2 [R11]	IO_L38N_0 [G13]	IO_L46P_2 [T10]	IO_L62N_0 [D19]
11	IO_L16P_2 [U14]	IO_L38P_0 [H13]	IO_L16N_2 [U13]	IO_L62P_0 [D18]
12	IO_L4N_2 [V15]	IO_L49P_0 [H14]	IO_L23N_2 [U15]	IO_L49N_0 [G15]
13	IO_L4P_2 [U16]	IO_L51N_0 [F17]	IO_L23P_2 [T15]	IO_L63N_0 [A18]
14	IO_L20P_2 [W14]	IO_L51P_0 [G16]	IO_L20N_2 [Y14]	IO_L63P_0 [B18]
15	IO_L5N_2 [Y18]	IO_L37N_GCLK12_0 [F16]	IO_L17N_2 [W15]	IO_L34N_GCLK18_0 [F10]
16	IO_L5P_2 [W17]	IO_L37P_GCLK13_0 [E16]	IO_L17P_2 [Y16]	IO_L34P_GCLK19_0 [G9]
17	GND	GND	GND	GND
18	IO_L15P_2 [Y17]	IO_L8N_0 [A5]	IO_L15N_2 [AB17]	IO_L6N_0 [A4]
19	IO_L21N_2 [AB15]	IO_L8P_0 [C5]	IO_L19N_2 [AB16]	IO_L6P_0 [C4]
20	IO_L21P_2 [Y15]	IO_L4P_0 [E5]	IO_L19P_2 [AA16]	IO_L4N_0 [E6]
21	IO_L6P_2 [AA14]	IO_L32N_0 [F9]	IO_L6N_2 [AB14]	IO_L7N_0 [F8]
22	IO_L18P_2 [V13]	IO_L32P_0 [G8]	IO_L18N_2 [W13]	IO_L7P_0 [F7]
23	GND	GND	GND	GND
24	IO_L40P_2 [W12]	GND	IO_L40N_2 [Y12]	IO_L36N_GCLK14_0 [F15]
25	IO_L30N_GCLK0_2 [AB13]	IO_L30P_GCLK1_2 [Y13]	IO_L32P_GCLK29_2 [Y11]	IO_L36P_GCLK15_0 [F14]
26	IO_L32N_GCLK28_2 [AB11]	GND	IO_L51P_1 [W20]	IO_L2N_0 [D5]
27	IO_L42N_2 [W11]	IO_L35N_GCLK16_0 [G11]	IO_L42P_2 [V11]	IO_L2P_0 [D4]
28	IO_L40P_GCLK11_1 [M20]	GND	GND	GND
29	3.3V	3.3V	3.3V	3.3V
30	0V	0V	0V	0V
31	AGND	AGND	AGND	AGND
32	AVNEG	AVNEG	AVPOS	AVPOS

Table 10: External Bus connector – FPGA signals

Expansion Port

The D.Module2 Expansion Port signals EXP-0 to EXP-32 are accessible on solder pads. Layout restrictions did not allow to fit a connector to these signals, however, you can solder wire connections to these pads if required.

Mechanics

Four M2.8 mounting holes are provided on the circumference of the board. These mounting holes are electrically connected to the shield of the I/O connectors and to the shield of the D.Module2 mounting holes.